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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,667	12/28/2001	Seung-Kyu Choi	3430-0172P	3666

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EXAMINER
LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,667	CHOI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *15-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 15-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

Claim Objections

Claim 6 is objected to because of the following informalities: it is suggested the limitation "a side surfaces" be replaced with "a side surface [surfaces]". Appropriate correction is required.

Claim 14 is objected to because of the following informalities: there is insufficient antecedent basis for "the passivation".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 7, 8, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regards to claims 3, 7, 8, and 12, the limitation "the same plane surface" renders the claims indefinite. It is unclear what is meant by this limitation. It cannot be determined how "the same plane surface" structurally distinguishes the claimed invention. Furthermore, there is insufficient antecedent basis for "the same plane surface".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6-9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US Pat. 6,091,466, hereinafter Kim '466).

In regards to claim 1, Figures 4 and 5F disclose of Kim '466 disclose an array substrate for a liquid crystal display device, comprising: a substrate 101; gate and data lines (113 and 123) crossing each other on the substrate; a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer 133, and source and drain electrodes (121 and 131) facing and spaced apart from each other; a passivation layer 137 over the gate and data

lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side surface of the drain electrode; and a pixel electrode 141 on the passivation layer.

In regards to claim 2, Figure 5F of Kim '466 discloses the pixel electrode 141 is electrically connected to the drain electrode through the contact hole.

In regards to claims 3 and 7, as best the examiner can ascertain the claimed invention, Figure 5F of Kim '466 discloses the semiconductor layer 133 has the same plane surface as the data line and the source and drain electrodes except for a portion between the source and drain electrodes.

In regards to claims 6 and 9, Figures 4 and 5F of Kim '466 disclose an array substrate for a liquid crystal display device, comprising: a substrate 101; gate and data lines (113 and 123) crossing each other on the substrate; a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer 133, a plurality of ohmic contact layers 135, and source and drain electrodes (121 and 131); a passivation layer pattern 137 on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surfaces of the drain electrode; and a pixel electrode 141 connected to the drain electrode.

In regards to claim 8, as best the examiner can ascertain the claimed invention, Figure 5F of Kim '466 discloses the plurality of ohmic contact layers have the same plane surfaces as the data line and the source and drain electrodes.

In regards to claim 12, as best the examiner can ascertain the claimed invention, Figures 4 and 5F of Kim '466 disclose an array substrate for a liquid crystal display device, comprising: a substrate 101; a gate line 113 on the substrate; a gate insulator 117 on the gate line; a semiconductor layer 133 on the gate insulator; a plurality of ohmic contact layers 135 on the

semiconductor layer; a data line 123 and a source and drain electrodes (121 and 131) on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode; a passivation layer 137 on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed; and a pixel electrode 141 connected to the drain electrode, the plurality of ohmic contact layers have the same plane surfaces as the data line and the source and drain electrodes, and wherein discloses the semiconductor layer 133 has the same plane surface as the data line and the source and drain electrodes except for a portion between the source and drain electrodes.

Claims 1, 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Akamatsu et al. (US Pat. 6,414,730, hereinafter Akamatsu).

In regards to claim 1, Figures 1 and 7A of Akamatsu disclose an array substrate for a liquid crystal display device, comprising: a substrate 51; gate and data lines (60 and 61) crossing each other on the substrate; a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer 54, and source and drain electrodes (58 and 59) facing and spaced apart from each other; a passivation layer 68 over the gate and data lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side surface of the drain electrode; and a pixel electrode 69 on the passivation layer.

In regards to claim 4, Figure 7A of Akamatsu discloses a gate insulation layer 53 formed underneath the passivation layer 68, wherein the contact hole is defined through the passivation layer and the gate insulation layer.

In regards to claim 5, Figure 7A of Akamatsu discloses the contact hole further exposes a portion of a top surface of the drain electrode.

Claims 6 and 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim.

In regards to claim 6, Figures 4 and 8 of Kim disclose an array substrate for a liquid crystal display device, comprising: a substrate 100; gate and data lines (130a and 150) crossing each other on the substrate; a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer 110, a plurality of ohmic contact layers (paragraph [0037]), and source and drain electrodes (150 and 170); a passivation layer pattern 160 on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surfaces of the drain electrode; and a pixel electrode 7 connected to the drain electrode. Note that Kim discloses in paragraph [0037] that the source and drain electrodes are in ohmic contact with the respective source and drain regions of the active layer 110, therefore it is considered that these source and drain regions are the ohmic contact layers.

In regards to claim 10, Figure 8 of Kim discloses a gate insulation film 120 over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film.

In regards to claims 11 and 14, Figure 8 of Kim discloses the passivation layer patter 160 further exposes a portion of a top surface of the drain electrode 170.

In regards to claim 12, as best the examiner can ascertain the claimed invention, Figures 4 and 8 of Kim disclose an array substrate for a liquid crystal display device, comprising: a substrate 100; a gate line 130a on the substrate; a gate insulator 120 on the gate line; a semiconductor layer 110 on the gate insulator; a plurality of ohmic contact layers on the

semiconductor layer (paragraph [0037]); a data line 150 and a source and drain electrodes (150 and 170) on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode; a passivation layer 160 on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed; and a pixel electrode 7 connected to the drain electrode, the plurality of ohmic contact layers have the same plane surfaces as the data line and the source and drain electrodes, and wherein discloses the semiconductor layer 133 has the same plane surface as the data line and the source and drain electrodes except for a portion between the source and drain electrodes. Note that Kim discloses in paragraph [0037] that the source and drain electrodes are in ohmic contact with the respective source and drain regions of the active layer 110, therefore it is considered that these source and drain regions are the ohmic contact layers.

In regards to claim 13, Figure 8 of Kim discloses a portion of the pixel electrode is formed directly on the gate insulator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (703) 305-4396.

The examiner can normally be reached from 8:00 AM-4: 30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or

proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew C. Landau

Examiner

June 8, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800